REMARKS

The Office Action mailed October 24, 2002, has been received and reviewed. Claim 10 has been cancelled, without prejudice or disclaimer. Claims 1-9 and 12-19 are currently pending in the application. Claims 1-9 and 12-19 stand rejected. Applicant has amended claims 1-3, 6, 13, 14, 16, and 19, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So.

Claims 1-3, 5-7, 10 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-3, 5-7, 10 and 12 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding amended independent claim 1, Applicants claim:

> A method for compressing video data in a computer system comprising:
> receiving a stream of data from a current video frame in the computer system, the computer system including a core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
> computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes **computing the difference frame in the core logic chip** within the computer system, wherein the core logic chip is a north bridge chip;
> **storing the difference frame in the system memory** in the computer system; and
> **the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data.** (Emphasis added.)

Regarding claim 1, Dea and So do not appear to teach or suggest "computing the difference frame in the core logic chip . . .; **storing the difference frame in the system memory** . . .; and the **host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data**", as claimed by Applicants.

Generally, Dea teaches of a "remote video processing system 100 including compression /decompression accelerator 120", (col. 4, lines 17-20), [wherein] "compression/decompression accelerator system 120 . . . ha[s] a straight pipeline architecture **rather than shared resources**" (col. 5, lines 24-29). More specifically, accelerator 120, as detailed in FIG. 2, includes:

1. a "frame difference block 220 [wherein] the information of reference frame line 209 [the "previous frame"] **is subtracted from** the current frame information on current frame line 205." (Col. 6, lines 37-40).
2. "A forward discrete cosine transform **is then performed on the data** from frame difference block 220 in encode dataflow 300 by forward discrete cosine transform block 230a." (Col. 10, lines 56-59; emphasis added).
3. "The transformed data from forward discrete cosine transform block 230a **is received by** quantization block 238 . . . **and quantized** therein. The quantized data from block 238 **is applied** by way of quantization output line 216 **to run length encoder** 246 for run length

encoding . . . [which] **are applied . . . to encode output circular buffer** 332 (see FIG. 3A) [with] [t]he data within encode output circular buffer 332 [] **then applied to variable length encoder** 112b to provide **compressed bit stream 338** [while] buffer 332 **may be located in memory 114 [the "system memory"**, see FIG. 1]." (Col. 10, line 65 through col. 11, line 11).

Clearly in Dea, the accelerator 120 includes substantial complexity as the difference frame undergoes significant compression processing within accelerator 120 before it is ever stored in the system memory. In fact, Dea teaches away from storing the data in the system memory by disclosing that "accelerator 120 of [Dea's] present invention within remote video interface system 100 ha[s] a straight pipeline architecture **rather than shared resources**." (See col. 5, lines 25-27; emphasis added.) Applicants claim, in amended independent claim 1, "computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . ; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data".

Regarding the So reference, the Office Action cites So because it "discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator [] is provide either at the North bridge or AGP graphic/video chip as described at column 17, lines 24-29." (See Office Action p. 3). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges. So engages in additional compression/decompression complexity within the North bridge and does not disclose "computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . ; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data", as claimed by Applicants in amended independent claim 1. Therefore, Applicants respectfully request that the rejection to claim 1, be withdrawn.

Regarding claim 2, the Office Action alleges that "the claimed storing the current video frame in the memory in the computer system is met by the current frame memory 204 (column 6, lines 42-44, and FIG. 2)." (See Office Action, p. 4.) Applicants respectfully disagree with the Examiner's characterization of the teaching of Dea. The citations accurately state "The difference between the reference frame data of line 209 and the current frame data of line 205 is then provided for encoding at the output of frame difference block 220. The information regarding the current frame line is received from bus interface 200 by way of current frame memory 204 and line 202."

Applicants respectfully assert that nothing within the four-corners of Dea discloses "storing the current video frame in the **system memory** in the computer system" as claimed by Applicants. In fact, a clear assemblage of the teachings of Dea prohibits the storage of the current video frame in the system memory. Referring to FIG. 2 of Dea, the current frame memory 204 is part of accelerator 120 which includes every element of FIG. 2. Referring now to FIG. 1 of Dea, accelerator 120 very independently couples to address bus 116 and data bus 118 which buses also couple to the "system memory" 114. Clearly, the current video frame 204 of Dea is not part of system memory 114. Therefore, since Dea and So, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 2, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 2 be withdrawn.

Regarding claim 3, the Office Action alleges that "the claimed wherein the current video frame is written over a previous video frame in the memory is met by the current frame memory 204 (column 6, lies 42-44, and FIG. 2.), whereas the current frame memory 204 receives video frame sequentially that the area stores the relatively previous video frame is subsequently replace by the newly received current video frame." (See Office Action, p. 4.) Applicants respectfully disagree with the Examiner's characterization of the teaching of Dea. The citations accurately state "The difference between the reference frame data of line 209 and the current frame data of line 205 is then provided for encoding at the output of frame difference block 220. The

information regarding the current frame line is received from bus interface 200 by way of current frame memory 204 and line 202."

Applicants respectfully assert that nothing within the four-corners of Dea discloses "wherein the current video frame is written over a previous video frame in the **system memory**" as claimed by Applicants. Applicants reaffirm the arguments from above that Dea prohibits the storage of the current video frame in the system memory. Therefore, since Dea and So, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 3, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 3 be withdrawn.

Regarding claims 5, Dea and So, either individually, or in any proper combination, do not appear to teach, suggest, or motivate Applicants' invention as a whole, as claimed in amended claim 5. Therefore, Applicants respectfully request that the rejection to claim 5 be withdrawn.

Regarding claim 6, Applicants sustain the above-arguments that nothing within Dea teaches of "storing the difference frame in the system memory" as claimed by Applicants in amended claim 6. Applicants reaffirm the arguments from above that Dea prohibits the storage of the difference frame in the system memory. Therefore, since Dea and So, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 6, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 6 be withdrawn.

Regarding claim 7, Dea and So, either individually, or in any proper combination, do not appear to teach, suggest, or motivate Applicants' invention as a whole, as claimed in Applicants' claim 7. Therefore, Applicants respectfully request that the rejection to claim 7 be withdrawn.

Regarding claim 10, Applicants have cancelled claim 10 without prejudice.

Regarding claim 12, Dea and So, either individually, or in any proper combination, do not appear to teach, suggest, or motivate Applicants' invention as a whole, as claimed in Applicants' claim 12. Therefore, Applicants respectfully request that the rejection to claim 12 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and further in View of U.S. Patent No. 4,546,383 to Abramatic.

Claims 4, 9, 13-17, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Abramatic (U.S. Patent No. 4, 546, 383). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 4, 9, 13-17, and 19 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claims 4, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claim 4. Applicants sustain the arguments above that nothing within the four-corners of the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 4 depends. Namely, Dea, So, and Abramatic do not teach, suggest, or motivate "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data . . . wherein computing the difference frame includes computing an exclusive-OR between the current video

frame and the previous video frame" as claimed in Applicants' claim 4. Therefore, Applicants respectfully request that the rejection to claim 4 be withdrawn.

Regarding claims 9, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claim 9. Applicants sustain the arguments above that nothing within the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 9 depends. Namely, Dea, So, and Abramatic do not teach, suggest, or motivate "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data . . . including using the video data in compressed form in a video teleconferencing system" as claimed in Applicants' claim 9. Therefore, Applicants respectfully request that the rejection to claim 9 be withdrawn.

Regarding amended independent claim 13, Applicants claim:

> A method for compressing video data in a computer system comprising:
> receiving a stream of data from a current video frame in the computer system, the computer system including a core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
> computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes **computing the difference frame in the core logic chip** within the computer system, wherein the core logic chip is a north bridge chip;
> **storing the difference frame in the system memory** in the computer system;
> **storing the current video frame in the system memory in the computer system;**
> **the host retrieving the difference frame directly from the system memory; and**
> **compressing the video data using the difference frame to produce compressed video data.** (Emphasis added.)

Dea, So, and Abramatic do not appear to teach or suggest "computing the difference frame in the core logic chip . . .; **storing the difference frame in the system memory** . . . **storing the current video frame in the system memory** . . .; and the **host retrieving the**

difference frame directly from the system memory . . . compressing the video data using the difference frame to produce compressed video data" as claimed by Applicants.

Generally as described above with regard to Dea, Dea teaches of a "remote video processing system 100 including compression /decompression accelerator 120", (col. 4, lines 17-20), [wherein] "compression/decompression accelerator system 120 . . . ha[s] a straight pipeline architecture rather than shared resources" (col. 5, lines 24-29). More specifically, accelerator 120, as detailed in FIG. 2, includes (i) a frame difference block 220; (ii) a **forward discrete cosine transform coupled to the frame difference block 220** wherein (iii) "[t]he transformed data from forward discrete cosine transform block 230a is received by quantization block 238 . . . and quantized therein. The quantized data from block 238 is applied by way of quantization output line 216 to run length encoder 246 for run length encoding . . . [which] are applied . . . to encode output circular buffer 332 (see FIG. 3A) [with] [t]he data within encode output circular buffer 332 [] then applied to variable length encoder 112b to provide **compressed bit stream 338** [while] buffer 332 **may be located in memory 114 [the "system memory"**, see FIG. 1]." (Col. 10, line 65 through col. 11, line 11).

Clearly in Dea, the accelerator 120 includes substantial complexity as the difference frame undergoes significant compression processing **within accelerator 120** before it is ever stored in the system memory. Applicants claim, in amended independent claim 13, "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . . and the host retrieving the difference frame directly from the system memory . . .; and compressing the video data using the difference frame to produce compressed video data."

Regarding the So reference, the Office Action cites So because it "discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator [] is provide either at the North bridge or AGP graphic/video chip as described at column 17, lines 24-29." (Office Action p. 3). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges.

Regarding Abramatic, the Office Action cites Abramatic alleging that "Abramatic et al. teaches that a form of video compression consists in detecting variations (difference) between on image and the next as describe at column 2, lines 53-56 [and that] Abramatic discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image a the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame." (See Office Action, pp. 10-11.) While Abramatic may disclose calculating a difference frame through the use of an exclusive-OR function, neither Dea, So, nor Abramatic, either individually or in any proper combination, teach suggest or motivate "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data", as claimed by Applicants in amended independent claim 13. Therefore, Applicants respectfully request that the rejection to claim 13, be withdrawn.

Regarding claim 14, the Office Action alleges that "the claimed wherein the current video frame is written over a previous video frame in the memory is met by the current frame memory 204 (column 6, lies 42-44, and FIG. 2.), whereas the current frame memory 204 receives video frame sequentially that the area stores the relatively previous video frame is subsequently replace by the newly received current video frame." (See Office Action, p. 11.) Applicants respectfully disagree with the Examiner's characterization of the teaching of Dea. The citations accurately state "The difference between the reference frame data of line 209 and the current frame data of line 205 is then provided for encoding at the output of frame difference block 220. The information regarding the current frame line is received from bus interface 200 by way of current frame memory 204 and line 202."

Applicants respectfully again assert that nothing within Dea discloses "wherein the current video frame is written over a previous video frame in the **system memory**" as claimed by Applicants. Applicants reaffirm the arguments from above that Dea prohibits the storage of

the current video frame in the system memory. Therefore, since Dea, So, or Abramatic, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 14, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 14 be withdrawn.

Regarding claim 15, Dea, So, or Abramatic, either individually, or in any proper combination, do not appear to teach, suggest, or motivate Applicants' invention as a whole, as claimed in Applicants' amended claim 15. Therefore, Applicants respectfully request that the rejection to claim 15 be withdrawn.

Regarding claim 16, Applicants sustain the above-arguments that nothing within Dea teaches of "storing the difference frame in the system memory" as claimed by Applicants in amended claim 16. Applicants reaffirm the arguments from above that Dea prohibits the storage of the difference frame in the system memory. Therefore, since Dea, So, and Abramatic, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 16, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 16 be withdrawn.

Regarding claim 17, Dea, So or Abramatic, either individually, or in any proper combination, do not appear to teach, suggest, or motivate Applicants' invention as a whole, as claimed in Applicants' claim 17. Therefore, Applicants respectfully requests that the rejection to claim 17 be withdrawn.

Regarding claim 19, the Office Action alleges that

> the system of Dea, So and Abramatic et al. discloses the claimed invention except for the claimed step of storing instruction and data for the computer system in the memory. Dea teaches a step of storing data from the computer system in the memory as the description of DRAM at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51).
> Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate process in common memories. (See Office Action , pp. 12-13.)

Applicants respectfully disagree with the characterization of Dea. A careful reading of Dea at the cited reference locations, namely column 4, lines 52-63, discloses that the accelerator 120 is "memory mapped" in a processor's address space, namely, "accelerator 120 is not required to decode all of the available one hundred twenty-eight kilobyte address space (see col. 4, lines 64-66)". Dea does NOT teach of accelerator 120 using "system memory" including "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data . . . [and] storing instructions and data . . . in the system memory", as claimed by Applicants in amended independent claim 19. In fact, Dea teaches away from storing the data in the system memory by disclosing that "accelerator 120 of [Dea's] present invention within remote video interface system 100 ha[s] a straight pipeline architecture **rather than shared resources**." (See col. 5, lines 25-27; emphasis added.) Therefore, since Dea, So, or Abramatic, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 19, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 19 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and Further in View of U.S. Patent No. 5,926,223 to Hardiman.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

> art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 8 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 8, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claim in claim 8, including all of the claim limitations of the base claim, namely, "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 8, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 8 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,926,223 to Hardiman.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S. Patent No. 4,546,383) and further in view of Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 18, Dea, So, Abramatic, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claim in claim 18, including all of the claim limitations of the base claim, namely, "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 18, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 18 be withdrawn.

ENTRY OF AMENDMENTS

The amendments to claims 1-3, 6, 13, 14, 16, and 19 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-9 and 12-19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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KKJ:ah
Date: January 24, 2003
Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Four-times Amended) A method for compressing video data in a computer system comprising:

receiving a stream of data from a current video frame in the computer system, the computer system including a core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing the difference frame in the [a] core logic chip within the computer system, wherein the core logic chip is a north bridge chip [that couples the processor to a main memory and a system bus for the computer system; and];

storing the difference frame in the system [a] memory in the computer system[.]; and

the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data.

2. (Amended) The method of claim 1, including storing the current video frame in the system memory in the computer system.

3. (Amended) The method of claim 2, wherein the current video frame is written over a previous video frame in the system memory.

6. (Amended) The method of claim 1, wherein storing the difference frame in memory includes storing the difference frame in the system memory using block transfers.

13. (Four-times Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system, the computer system including a core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in the [a] core logic chip within the computer system, wherein the core logic chip is a north bridge chip[that couples the processor to a main memory and a system bus for the computer system];

storing the difference frame in the system [a] memory in the computer system;

storing the current video frame in the system memory in the computer system;[and]

the host retrieving the difference frame directly from the system memory; and

compressing the video data using the difference frame to produce compressed video data.

14. (Amended) The method of claim 13, wherein the current video frame is written over a previous video frame in the system memory.

16. (Amended) The method of claim 13, wherein storing the difference frame in system memory includes storing the difference frame in the system memory using block transfers.

19. (Amended) The method of claim 13, including storing instructions and data for the computer system in the system memory.